PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Serial No. 10/798,657
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09/05/2006 /Pamela Gerik/
Date Pamela Gerik

SUPPLEMENTAL APPEAL BRIEF

Sir/Madam:

This Supplemental Appeal Brief is presented in response to the Notice of Non-Compliant Brief Mailed August 4, 2006. The original Appeal Brief was filed further to the Notice of Appeal filed May 12, 2006. The Notice of Appeal was filed following receipt of a final Office Action mailed February 14, 2006. Appellant hereby appeals to the Board of Patent Appeals and Interferences from a final rejection of claims 1-4, 6, 8-16, 18, and 19, as well as the objection to claim 17, and respectfully requests that this appeal be considered by the Board.

I. REAL PARTY IN INTEREST

The subject application is owned by Cypress Semiconductor Corp. as evidenced by the assignment recorded at reel 015078 and frame 0195.

II. RELATED APPEALS AND INTERFERENCES

No appeals, interferences, or judicial proceedings are known which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-4, 6, and 8-19 are pending and hereby appealed. Claims 5 and 7 are canceled. Claims 1-4, 6, 8-16, 18, and 19 stand rejected, and claim 17 is objected to as being dependent upon a rejected base claim.

IV. STATUS OF AMENDMENTS

No amendments to the claims were filed subsequent to their final rejection. Therefore, the Appendix hereto reflects the current state of the claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed subject matter generally relates to a circuit, system, and method of translating low voltage differential signals (LVDS) into higher voltage swings (Specification -- pg. 1, line 24 - pg. 2, line 13). However, in order to accurately translate the differential signals, a consistent time delay is required across differing transitional edges of the incoming signal (Specification -- pg. 3, lines 9-12). Specifically, the delay on both the rising and falling edges (t_{d1} and t_{d2}) must be consistent and equal for each transition (Specification -- pg. 3, lines 17-21; Fig. 2). To achieve consistent time delays for each rising and falling transition, an AC coupling capacitor, an inverter, and a biasing circuit, according to one embodiment of the present invention is coupled to each of the differential pair outputs (Specification -- pg. 5, lines 8-13). The differential amplifier 32 has differential outputs (D^+ and D^-) coupled to a pair of capacitors 34, which are then coupled to a pair of inverters 36a/36e, and a biasing circuit is coupled between capacitors 34 and inverters 36a/36e (Specification -- pg. 9, lines 6-21; Fig. 3).

According to that described in independent claim 1, the biasing circuit 38 can comprise a transmission gate having a p-channel transistor coupled in parallel with an n-channel transistor (Specification -- pg. 10, lines 24-26; Figs. 3-4). In addition to its normal operational mode, the biasing circuit can be powered down by applying a power supply voltage to the gate terminal of the p-channel transistor and a ground supply voltage to the gate of the n-channel transistor (Specification -- pg. 10, line 28 - pg. 11, line 7). A power down (PD) signal containing the

power down voltage placed at a power supply voltage value is applied to the gate terminal of the p-channel transistor, and an inverter 40 is used to place the complementary voltage value on the n-channel transistor (Specification -- Figs. 3-4). Claim 1 illustrates placement of the biasing circuit in a power down mode by correspondingly placing the transmission gate in an "open" status condition (Specification -- pg. 10, line 30 - pg. 11, line 2). It is not merely an obvious design choice to open a transmission gate which has one end of the transmission gate coupled to an input of a high gain amplifier 36a/36e. If the gate terminal of the amplifier is open and merely floating, the amplifier will go into an unpredictable state possibly causing the benefit of a power down status to be lost. A power down circuit 40 is utilized to prevent this occurrence.

The invention set forth in independent claim 18 not only describes biasing of an inverter, coupling onto an inverter an alternating current (AC), and switching the inverter output depending on the coupled AC component, but most importantly describes removing the biasing at a specific time (Claim 18, last element). Removing the biasing involves driving the biasing at the input of inverter 36a/36e to a ground supply voltage (Claim 18, last element). A power down circuit 40 is duplicated on both complementary outputs from differential amplifier 32 (Specification -- pg. 9, lines 6-11; Figs. 3-4). Power down circuit 40 receives the power down (PD) signal, which in this case is a logic high voltage value, and in response drives node 42a/42b to a ground supply. This prevents the input to the high gain amplifiers 36a/36e from floating whenever the bias circuit is in an "open" status condition. Thus, claim 18 further describes the power down circuit applied to the inputs of amplifiers 36a/36e whenever the bias circuit is powered down according to claim 1.

The invention set forth in independent claim 11 derives from recognizing the full complementary circuitry of a pair of inverters, a pair of biasing circuits, and a pair of capacitors coupled to the differential amplifier complementary outputs. Specifically, claim 11 replicates the translational circuitry on both differential outputs to formulate a dual-ended receiver circuit, as opposed to a single-ended circuit. While a dual-ended circuit involves added circuitry, a dual-ended receiver is necessary in order to achieve consistent rise and fall times on the differential output (Specification -- pg. 3, line 23 - pg. 4, line 2).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-4, 6, 8-16, 18, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,906,871 to Iida (hereinafter "Iida").

VII. ARGUMENT

The contentions of the Appellant with respect to the ground of rejection presented for review, and the basis thereof, with citations of the statutes, regulations, authorities, and parts of the record relied upon are presented herein for consideration by the Board. Details as to why the rejections cannot be sustained are set forth below.

A. Rejection of Claims 1-4, 6, 8-16, 18, and 19 under 35 U.S.C. § 103(a)

Claims 1-4, 6, 8-16, 18, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,906,871 to Iida (hereinafter "Iida"). To establish a case of *prima facie* obviousness of a claimed invention, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Second, there must be a reasonable expectation of success. As stated in MPEP 2143.01, the fact that references can be hypothetically combined or modified is not sufficient to establish a *prima facie* case of obviousness. *See In re Mills*, 916 F.2d. 680 (Fed. Cir. 1990). Finally, the prior art references must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d. 981 (CCPA 1974); MPEP 2143.03, emphasis added. Specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d., 1382 (CCPA 1970). Using these standards, Applicants contend that the cited art fails to teach or suggest all features of the currently pending claims, some distinctive features of which are set forth in more detail below.

Iida does not suggest or provide motivation for a transmission gate having a gate terminal of a p-channel transistor coupled to a power supply voltage and a gate terminal of a n-channel transistor coupled to a ground supply voltage during power down of the circuit. Independent claim 1 recites in part:

> A circuit, comprising . . . a biasing circuit comprising a transmission gate that includes a p-channel transistor coupled in parallel with a n-channel transistor between the capacitor and the inverter, wherein a gate terminal of the p-channel transistor is coupled to a power down voltage at a power supply voltage and a gate terminal of the n-channel transistor is coupled to a ground supply voltage during power down of the circuit.

Independent claim 1 specifically recites power down of the biasing circuit by coupling a gate terminal of the p-channel transistor to a power supply voltage and a gate terminal of the n-channel transistor to a ground supply voltage. Specifically, the p-channel transistor gate terminal is coupled to a power supply voltage and the n-channel transistor gate is coupled to a ground supply voltage during a specific time known as the power down time.

Contrary to claim 1, Iida specifically discloses the opposite to that which is claimed. For example, Iida denotes the p-channel transistor Q8 is coupled to a ground supply voltage, and the n-channel transistor Q7 is coupled to a power supply voltage (Iida -- Fig. 7). As further described in Iida, in order to form a bias resistor R5, both transistors Q7 and Q8 must be in a conductive state (Iida -- col. 4, lines 62-66). In order to place transistors Q7 and Q8 in a conductive state, the p-channel transistor must have its gate grounded and the n-channel transistor must have its gate connected to a power supply (Iida -- col. 4, lines 34-44). The teachings of Iida that the n-channel transistor gate be coupled to a power supply and the p-channel transistor gate be coupled to a ground supply is exactly the opposite of that which is presently claimed. The purpose of Iida is to render the transistors of the transmission gate conductive. No motivation is provided anywhere in Iida for reversing the conductive state of those transistors and, specifically, to reverse the conductive state of the transistors during a power down timeframe.

Iida must suggest the desirability of the present claims or must at least show to a skilled artisan a motivation to modify Iida to arrive at present claim 1. MPEP 2143.01. Absent any suggestion or motivation in Iida and, in fact, when it teaches away from the present claim 1, Iida cannot be used to support a *prima facie* case of obviousness. Essentially, teaching away from the art is a *per se* demonstration of lack of *prima facie* obviousness. *In re Dow Chemical Co.*, 837 F.2d. 469 (Fed. Cir. 1988). When examining Iida, a skilled artisan would maintain the transmission gate always in the conductive state and would not be motivated to modify that state at any time, and certainly would not be motivated to render the transmission gate in a non-conductive state during a power down operation.

The requirement that Iida forms a bias resistor R5 by placing transistors Q7 and Q8 in a conductive state flies in the face of what is currently claimed during power down in which the transistors of a transmission gate are placed in an "open" state. A skilled artisan would certainly know the difference between an open state and a conductive state, and would further know that Iida requires that transistors Q7 and Q8 be in a conductive state at all time. Iida does not make any accommodation for placing the transmission gate in an open state, nor does Iida make recommendations for what would occur to the input of the inverter 20 if somehow, hypothetically, a power down state were to exist somewhere in the teachings Iida. Instead, Iida requires a biasing resistor R5 be of relatively low value in order for the output and input of the inverter 20 be near its trip point and in a maximum gain state (Iida -- col. 3, lines 18-21). If bias resistor R5 no longer exists and is instead replaced by an open circuit, CMOS inverter 20 no longer is provided with "a predetermined bias voltage to the input node" as required in Iida (Iida -- col. 3, lines 38-41). Therefore, Appellants disagree with characterizations made in the final Office Action that it would be a mere obvious design choice to rearrange the logic levels of the gates of p-channel and n-channel transistors. Not only is Iida lacking such a suggestion, but to do so would defeat the purpose of using resistor R5 as a bias circuit. Accordingly, Appellants assert that independent claim 1 and claims dependent therefrom are not obvious over Iida.

Iida does not suggest or provide motivation for a biasing circuit coupled to an input of each of a pair of inverters, or a pair of capacitors coupled between the pair of inverters and the respective pair of outputs of a differential amplifier. Present claim 11 recites in part:

> A receiver, comprising . . . a pair of inverters; a biasing circuit coupled to an input of each of the pair of inverters . . . a differential amplifier adapted to receive a differential input signal . . . and a pair of capacitors coupled between the pair of inverters and respective pair of outputs of the differential amplifier to place upon each of the pair of inverters changes in voltage centered around the trip point, wherein the changes in voltage correspond to changes in amplitude of the differential input signal.

Independent claim 11 describes a dual-ended embodiment in which the complementary outputs of the differential amplifier are coupled to a pair of inverters, a pair of biasing circuits, and a pair of capacitors having a dual-ended receiver with a dual-ended translation circuitry. This embodiment eliminates duty cycle distortion at four different points in time on each of the complementary outputs. Those four different points of time are described in the present specification as to each of the differential pair output (Specification -- pg. 4, lines 4-14).

Contrary to the dual-ended features of claim 11, Iida only teaches use of a single-ended output from resistor R3. Thus, only a single capacitor, a single inverter, and a single biasing circuit is shown, described, or suggested in Iida (Iida -- Fig. 3). In fact, Iida specifically teaches away from replicating the circuit to provide a dual-ended output, since the purpose of Iida is to "provide a level shift circuit which requires a reduced number of circuit elements" compared to that of the prior art circuit of Fig. 1 which has a dual-ended output, but absent a biasing circuit and capacitor at each output (Iida -- col. 1, lines 54-56, emphasis added; Figs. 1 and 3 in comparison). Moreover, Iida explicitly states that "it is noted here that the level shift circuit is made up of only capacitor 19, CMOS inverter 20, and the bias circuit or resistor R5" (Iida -- col. 4, lines 18-21, emphasis added). Iida continues by noting the level shifter of Fig. 3, when compared to that shown in Fig. 1, requires less number of circuit elements -- the primary goal of Iida (Iida -- col. 4, lines 22-25).

Since Iida appears to specifically require only a single-ended output with fewer circuit elements, nowhere in Iida is there any suggestion for modifying its purpose to having a dual-ended output with more circuit elements. Accordingly, Appellants assert that independent claim 11 and claims dependent therefrom are not obvious over Iida.

Iida does not suggest or provide motivation for removing the biasing and driving the biasing to a ground supply voltage during times when the differential signal is absent. Present claim 18 recites in part:

> A method for translating voltages of a differential signal to complementary metal oxide semiconductor (CMOS) voltages, comprising: biasing an input of a CMOS inverter . . . coupling onto the CMOS inverter an alternating current (AC) . . . switching the inverter output to CMOS voltage levels . . . and removing the biasing and driving the biasing to a ground supply voltage during times when the differential signal is absent.

Not only does present claim 18 remove biasing by placing transmission gate 38 in an "open" status with PD drawn to a power supply voltage, but also activates the power down circuit 40 by placing transistor 40 in a conductive state (Specification -- Figs. 3-4). By removing the biasing that would normally be applied by transmission gate 38 and driving the biasing at node 42a/42b to ground via transistor 40, claim 18 makes clear that the input to amplifier 36a/36e is pulled to ground and not floating -- a deleterious circumstance in CMOS devices. Thus, when the differential signal is absent, the combination of circuits 38 and 40 remove the biasing and drive the biasing to a ground supply voltage. Specifically, present Fig. 3 illustrates a CMOS inverter 36a/36e that is biased to a ground supply via transistor 40 (Specification -- Fig. 3). Nowhere is there any suggestion in Iida for biasing the input of inverter 20 to a ground supply during times when a differential signal is absent (Iida -- Fig. 3). Accordingly, Applicants assert that independent claim 18 and claims dependent therefrom are not obvious over Iida.

For the foregoing reasons, it is submitted that the Examiner's rejection of and/or objection to claims 1-4, 6, 8-16, 18, and 19, as well as the objection to claim 17, was erroneous, and reversal of the Examiner's decision is respectfully requested.

The Commissioner is hereby authorized to charge the required fee(s) to deposit account number 50-3268/5298-13101.

Respectfully submitted,
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VIII. APPENDIX

The present claims on appeal are as follows.

1. A circuit, comprising:

a differential amplifier;

a capacitor coupled to an output of the differential amplifier;

an inverter coupled to the capacitor; and

a biasing circuit comprising a transmission gate that includes a p-channel transistor coupled in parallel with a n-channel transistor between the capacitor and the inverter, wherein a gate terminal of the p-channel transistor is coupled to a power down voltage at a power supply voltage and a gate terminal of the n-channel transistor is coupled to a ground supply voltage during power down of the circuit.

2. The circuit as recited in claim 1, wherein the inverter comprises a p-channel transistor coupled in series with an n-channel transistor.

3. The circuit as recited in claim 1, wherein the capacitor comprises a pair of conductive terminals separated by a dielectric, and wherein a first terminal of the pair of terminals is coupled to the output of the differential amplifier and a second terminal of the pair of terminals is coupled to the inverter.

4. The circuit as recited in claim 1, wherein the inverter comprises a terminal coupled to the capacitor.

6. The circuit as recited in claim 1, wherein a gate terminal of the p-channel transistor is coupled to the power down voltage at a ground supply voltage and a gate terminal of the n-channel transistor is coupled to the power supply voltage during operation of the circuit.

8. The circuit as recited in claim 1, wherein the biasing circuit comprises a second inverter.

9. The circuit as recited in claim 8, wherein the second inverter comprises both an input and an output coupled to the capacitor.

10. The circuit as recited in claim 8, wherein the inverter comprises a first p-channel transistor and an first n-channel transistor having substantially the same gate length but having a first p-channel gate width at a first ratio relative to first n-channel gate width, and wherein the second inverter comprises second p-channel transistor and a second n-channel transistor having substantially the same gate length but having a second p-channel gate width at a second ratio relative to a second n-channel gate width, and wherein the first ratio is approximately equal to the second ratio.

11. A receiver, comprising:

a pair of inverters;

a biasing circuit coupled to an input of each of the pair of inverters to bias a voltage on the pair of inverters to a trip point of the inverters;

a differential amplifier adapted to receive a differential input signal forwarded to the receiver from a transmission medium; and

a pair of capacitors coupled between the pair of inverters and respective pair of outputs of the differential amplifier to place upon each of the pair of inverters changes in voltage centered around the trip point, wherein the changes in voltage correspond to changes in amplitude of the differential input signal.

12. The receiver as recited in claim 11, wherein each of the pair of inverters is a complementary metal oxide semiconductor (CMOS) inverter.

13. The receiver as recited in claim 11, wherein the biasing circuit comprises a transmission gate coupled between the input and output of each of the pair of inverters to maintain a direct current (DC) voltage bias on the input of each of the pair of inverters approximately at the trip point of the inverters.

14. The receiver as recited in claim 11, wherein the transmission gate comprises a p-channel transistor coupled in parallel with an n-channel transistor, wherein, during operation, a gate terminal of the p-channel transistor is coupled to a power down voltage at a ground supply voltage and a gate terminal of the n-channel is coupled to a power supply voltage, and wherein during non-operation, the gate terminal of the p-channel transistor is coupled to the power down voltage at a power supply voltage and a gate terminal of the n-channel is coupled to the ground supply voltage.

15. The receiver as recited in claim 11, wherein the biasing circuit comprises a second inverter having an input coupled to an output of the inverter and also having an output coupled to an input of the inverter.

16. The receiver as recited in claim 15, wherein the ratio of gate widths p-channel and n-channel transistors of the inverter and the second inverter are substantially equal.

17. The receiver as recited in claim 15, wherein the second inverter comprises a four-input inverter, with two inputs coupled to receive a power supply voltage and a ground supply voltage.

18. A method for translating voltages of a differential signal to complementary metal oxide semiconductor (CMOS) voltages, comprising:

biasing an input of a CMOS inverter to a trip point at which a voltage on the input of CMOS inverter substantially equals a voltage on the output of the CMOS inverter;

coupling onto the CMOS inverter an alternating current (AC) component of the differential signal absent a direct current (DC) component of the differential signal;

switching the inverter output to CMOS voltage levels whenever the AC component causes the voltage on the biased input of the CMOS inverter to exceed or become less than the trip point of the inverter; and

removing the biasing and driving the biasing to a ground supply voltage during times when the differential signal is absent.

19. The method as recited in claim 18, wherein the biasing comprises maintaining a previous AC component of the differential signal onto the biased input of the CMOS inverter during times when the differential signal is removed.

IX. EVIDENCE APPENDIX

No evidence has been entered during the prosecution of the captioned case.

X. RELATED PROCEEDINGS APPENDIX

No prior or pending appeals, interferences, or judicial proceedings are known to Appellant or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.